

6th International Conference on Silicon Photovoltaics, SiliconPV 2016

Plasma-free dry-chemical texturing process for high-efficiency multicrystalline silicon solar cells

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Abstract

In this paper, we study the influence of modifying the geometry of nanotexture on its electrical properties. Nanotexture is formed by an industrially feasible dry-chemical etching process performed entirely in atmospheric pressure conditions. A surface modification process is developed that allows low surface recombination velocities ($S_{\text{eff,min}} \leq 10 \text{ cm/s}$) on nanotextured surfaces. By simultaneously improving the surface passivation and the emitter diffusion processes, we achieve an equivalent passivation level ($V_{\text{OC,impl}} \geq 670 \text{ mV}$) for nanotextured surfaces to that of reference textured surfaces after applying either PECVD or ALD based deposition techniques.

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Peer review by the scientific conference committee of SiliconPV 2016 under responsibility of PSE AG.

Keywords: black silicon; atmospheric pressure; dry texturing; silicon nitride; surface passivation; emitter recombination

1. Introduction

Higher surface reflection of multicrystalline silicon (mc-Si) wafers is one of the major reasons for an overall lower conversion efficiency of mc-Si based solar cells in comparison to monocrystalline silicon (mono-Si) based solar cells. Formation of submicron or nano-scale texture in mc-Si significantly enhances its light trapping properties [1–3] and promises a significant increase in conversion efficiencies of mc-Si based solar cells [4–8]. Nano-scale

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texturing has been achieved by using various texturing mechanisms and especially plasma-based texturing; metal-assisted wet-chemical etching and laser-based texturing are mainly reported by the contemporary works [4,5,9–11]. We proposed a novel texturing approach of applying a plasma-free dry-chemical etching of Si in atmospheric pressure conditions by applying spontaneous F_2 -Si etching process and using an inline etching tool that promises industrial throughputs. The proposed atmospheric pressure dry etching (ADE) process forms nanostructures in a single-step process and especially is of high interest to significantly reduce the surface reflection of mc-Si wafers to a value close to or below that of alkaline textured mono-Si surfaces. In past, we showed that a shallow single-step ADE process can lead to an improvement in the short circuit current density (J_{sc}) and the conversion efficiency (η) of mc-Si based solar cells in comparison to the reference acidic textured solar cells [6]. The parameters of the ADE process can be also adjusted to form deep nanostructures or ‘black silicon (B-Si)’ structures with very low surface reflection values ($R_w < 3\%$). Here, the weighted surface reflection (R_w) is calculated in the wavelength spectrum of 300–1200 nm and a weighing function is applied using the internal quantum efficiency of a standard silicon solar cell under AM 1.5G illumination conditions [12]. An enlarged surface of B-Si, however, poses major challenges in surface passivation and emitter formation process steps. Therefore, optimization of all these process steps is necessary in order to achieve the maximum current gain promised by the low surface reflection of nanotextured surfaces. Surface modification of B-Si structures either by alkaline [4,7,8] or acidic [5,13] wet-chemical solutions is one of the approaches that have been applied to relax the influence of surface topography on the electrical characteristics of the nanotextured solar cells. Recently, we also showed that a short alkaline surface modification of the nanostructures formed after ADE process is fully compatible with plasma enhanced chemical vapor deposition (PECVD) based deposition process by achieving a conversion efficiency of 18.0 % on the mc-Si based Al-BSF solar cell [14]. Improvement in the solar cell performance by performing nanotexturing on mc-Si substrate has paved the way to incorporate this approach with high efficiency solar cell concepts like passivated emitter and rear cell (PERC). In high-efficiency solar cells like PERC, however, the limit imposed on open circuit voltage ($V_{OC,max}$) due to the recombination channels activated in a solar cell becomes much more important. Therefore, the surface passivation and emitter diffusion processes on nanotextured substrates have to be further optimized in order to allow high V_{OC} values that are promised by the high-efficiency solar cell architectures.

In this paper, we will therefore discuss about the important technological milestones achieved by us in order to pave the path towards high-efficiency PERC solar cells on nanotextured mc-Si substrates. We first discuss about our surface texturing approach by explaining the process development of the modified nanotexture (mB-Si) structures on c-Si surfaces. Based on the lifetime measurements of the un-diffused and diffused surfaces, we would then discuss in detail about the electrical characteristics of the mB-Si structures.

2. Process development

For this work, we use the atmospheric pressure dry-chemical etching tool developed by Nines Photovoltaics and installed at Fraunhofer ISE facility. Fig. 1 i) shows a basic schematic of the etching system. The texturing of c-Si surfaces is performed by spontaneous etching of the Si surfaces with dilute F_2 gas (F_2/N_2) in atmospheric pressure conditions. The wafers are then dynamically transferred through the reactor with a set velocity (v_{wafer}) in an inline mode. The temperature of the etching gas (T_{GDP}) and the Si wafer (T_{wafer}); total gas flux, F_2 concentration and v_{wafer} are the major process parameters that are varied to form nanostructures of different morphologies and aspect ratios. More about the set-up of the etching tool and the process mechanism can be read elsewhere [6,15,16].

Fig. 1 ii) show the experimental plan followed during the development of mB-Si texture. p-type 15.6 x 15.6 cm² mono c-Si (CZ) wafers are first saw-damage etched and then textured by flowing F_2 gas over the heated wafer ($T_{wafer} \approx 170^\circ\text{C}$), which is moved through the reaction chamber. The etching process parameters are varied to obtain black silicon (B-Si) -like topography. In order to modify the surface topography, the B-Si wafers are then shortly dipped into the diluted alkaline solution using an industrial batch wet-chemical tool from Stangl. We chose alkaline solutions after considering their higher Si etching rate in comparison to the acidic solutions for an equivalent concentration. Typical alkaline solutions like KOH/TMAH react with Si in a redox reaction where the hydroxyl (OH) dissolve Si in the form of $Si_x(OH)_y$ [17]. Assuming homogeneous etching of Si along the wafer area, we estimate Si removal based upon the weight measurements performed before and after the surface modification process. The hemispherical surface reflections are measured by Varian Cary 5000 spectrophotometer and the

morphology of the texture is investigated by scanning beam electron microscopy (SEM) measurements (Hitachi SU-70).

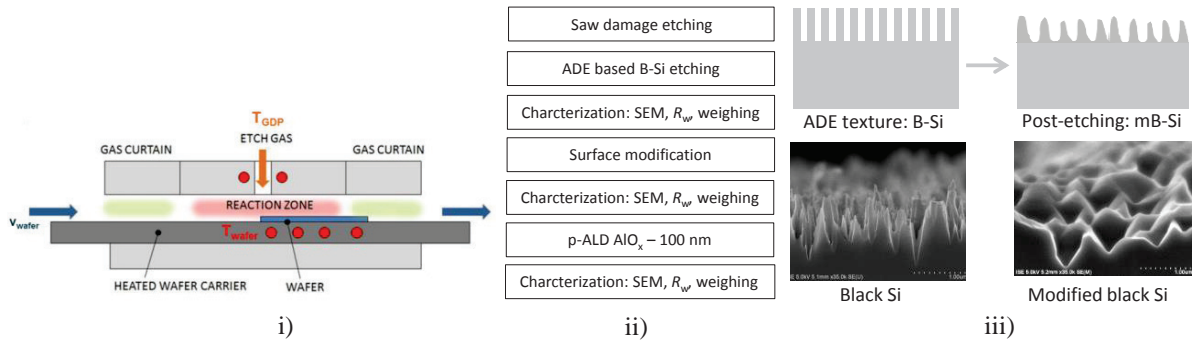


Fig. 1. i) Schematic of the atmospheric pressure dry etching (ADE) system installed at Fraunhofer ISE, ii) Experimental plan followed for the process development of mB-Si, iii) Impression and representative SEM images of the two-step texturing process of modifying black silicon texture obtained by ADE into modified black silicon (mB-Si).

In order to quantify the change in surface morphology of the nanostructures for different surface modification times, we estimate surface enlargement factors (S_f) for each surface texture and compare it to that of an ideal alkaline texture. In order to estimate S_f , 100 nm AlO_x is deposited on textured wafers by using a spatial fast atomic layer deposition (ALD) system that applies a principle of spatial separation of the half reactions – precursor adsorption and oxidation steps by moving the Si wafer through the respective reaction zones using the gas bearings [18]. ALD deposition is especially chosen to guarantee conformability of the deposited layer on the textured surfaces [19,20]. Based upon the assumption of homogeneous etching conditions in the wafer area and a perfectly conformal deposition of AlO_x layer on textured surface, S_f is calculated by estimating the enlarged area of the AlO_x layer on textured surface in comparison to a known area of the planar surface.

$$A_1 = \frac{\Delta m}{(\rho \times t)} \quad (1)$$

$$S_f = \left(\frac{A_1 - A_2}{A_2} \right) \times 100 \quad (2)$$

Where, ρ is the density of Al_2O_3 , t the thickness of the deposited layer, Δm the weight difference of wafer after deposition of 100 nm AlO_x layer, A_1 the estimated total surface area of textured surface, and A_2 the known total surface area of the non-textured Si wafer.

The volume of Si in the B-Si structure gradually decreases from the base and towards the tip that provides it a graded refractive index effect. The goal of the surface modification is to remove the thinner volume located in the top-section of the B-Si structure so as to simultaneously increase the width and to decrease the depth of the B-Si structures whereas still maintaining reasonably low surface reflection values. For such submicron structures, it has been reported that altering the dimensions of the structures (depth and period/width) has a strong influence in surface reflection values [21]. By maintaining a dilute concentration of the alkaline solution at a temperature close to the room temperature, the Si removal can be effectively controlled by varying the surface modification time. Fig. 1 iii) shows SEM image of a typical B-Si surface formed after ADE process and of mB-Si surface formed after a surface modification time of 90 s.

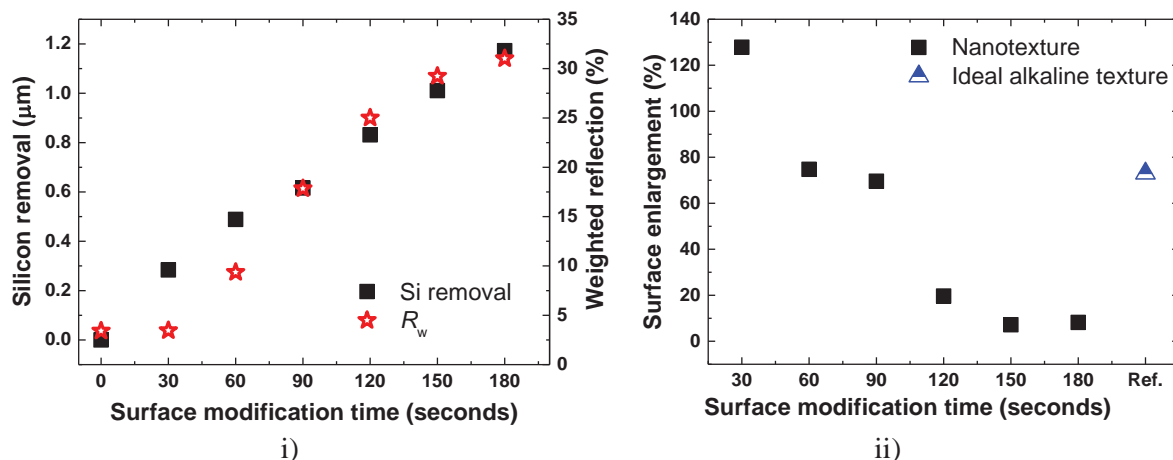


Fig. 2. Plot showing i) increasing Si removal and R_w , and ii) estimated percentage surface enlargement (S_f) of modified nanostructures for an increasing surface modification time of B-Si structures formed by ADE nanotexturing process.

Fig. 2 i) plots the amount of Si removal and estimated R_w after performing a variation of surface modification time on B-Si structures formed on mono c-Si surfaces by ADE process. As expected, Si removal increases almost linearly with an increasing surface modification time whereas R_w increases very slowly till 30 s, and then increases faster up to 150 s after which it is expected to saturate at $R_w \approx 30$ %. Fig. 2 ii) plots S_f for different nanotextured surfaces and compares it to that of an ideal alkaline texture ($S_f = 73$ %). It can be observed that a large surface enlargement of the B-Si surfaces ($S_f > 120$ %) dramatically reduces to that of an ideal pyramid texture after 60 s of the surface modification time. For an equivalent surface modification time, R_w increases from ≈ 3 % for B-Si surface to ≈ 10 % and ≈ 17 % for the mB-Si surfaces formed after 60 s and 90 s respectively. Nevertheless, these R_w values are much lower in comparison to the acidic textured surfaces and after deposition of PECVD SiN_x , a reasonably low R_w of < 4 % is achievable for both surface modification times of 60 s and 90 s.

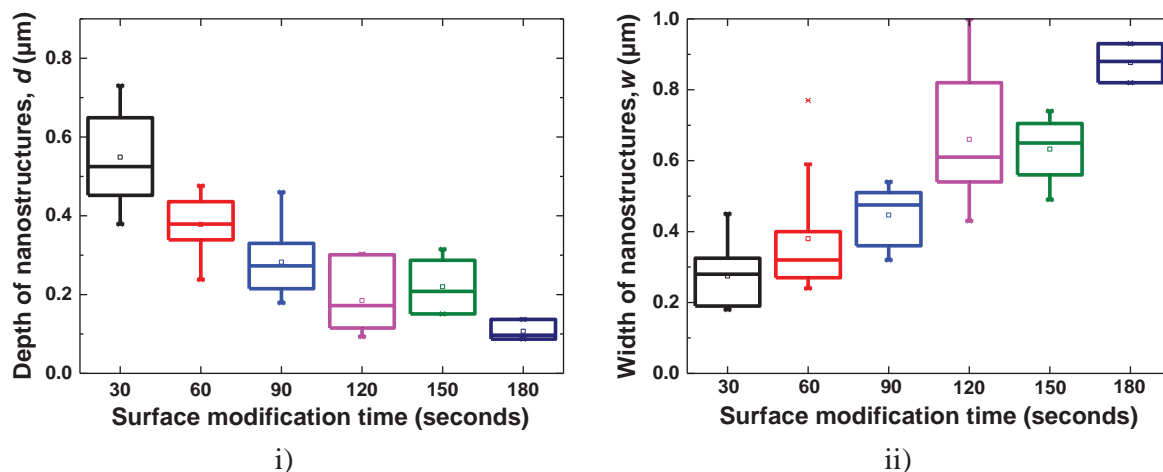


Fig. 3. Plot shows i) a decreasing depth, and ii) an increasing width of ADE nanostructures for an increasing surface modification time. The depths and widths are estimated from representative SEM images of the particular surface texture and therefore the measurements assist to make only a qualitative conclusion.

In Fig. 3 i) and ii), cross-sectional SEM images are used to estimate the depth and the width of modified nanostructures formed after varying surface modification times. Although the measurements performed on SEM images are prone to manual errors and therefore should not be considered as the absolute values, a general trend of an increment in surface reflection with an increasing width and a decreasing depth of nanostructures can be traced from these measurements. In the next subsection, influence of the surface modification on the electrical characteristics of nanostructures is discussed in detail.

3. Electrical characteristics of nanotextured surfaces

3.1. Surface passivation

A change in the surface topography of B-Si texture after the subsequent surface modification process is expected to allow more conformal deposition of dielectric surface passivation layers, especially if PECVD deposition method is applied. In this section, we investigate the influence of surface modification process on the surface recombination of nanotextured surfaces by applying both ALD and PECVD based surface passivation layers.

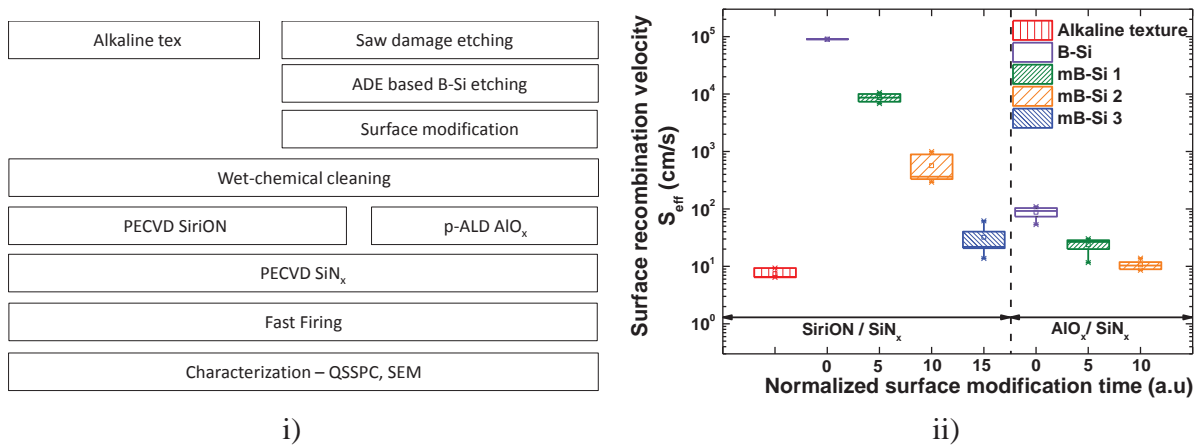


Fig. 4. i) Process plan followed for estimating carrier lifetimes nanotextured and reference textured surfaces after surface passivation and fast firing steps, ii) plot showing effective surface recombination velocity S_{eff} for nanotextured and reference textured surfaces.

Fig. 4 i) shows the process plan followed for the experiment. p-type, $4 \Omega \text{ cm}$ $15.6 \times 15.6 \text{ cm}^2$ CZ wafers of $200 \mu\text{m}$ starting thickness are first saw damage etched in an alkaline solution and then etched by ADE process on both sides to form B-Si texture ($R_w \approx 3\%$). Afterwards, the surface modification time for B-Si texture is varied in a linear fashion to form modified nanostructures with different surface reflection properties – mB-Si 1 ($R_w \approx 11 - 11.5\%$), mB-Si 2 ($R_w \approx 14-14.5\%$), and mB-Si 3 ($R_w \approx 17-17.5\%$). For reference, alkaline textured ($R_w \approx 11\%$) samples are also processed in parallel. The symmetrically textured samples are wet-chemically cleaned in HF/HNO_3 based solution before the surface passivation step. A group of nanotextured (B-Si and mB-Si) samples and all reference textured samples are coated on both sides by a layer stack of SiriON (20 nm) / SiN_x (60 nm) as described in [22]. The other group of nanotextured samples are deposited with a layer stack of AlO_x (10 nm) / SiN_x , with thickness of SiN_x adjusted to reach the reflection minimum at 600 nm. AlO_x is deposited by plasma-based atomic layer deposition (p-ALD) process (OpAL, Oxford Instruments) whereas both SiriON and SiN_x are deposited by PECVD process (Roth & Rau, SiNA). SiriON stack was chosen instead of SiN_x layer as it offers much higher carrier lifetimes on un-diffused samples [22]. In order to reach the maximum passivation level offered by PECVD SiriON stack as reported in [22], we chose 700°C as the firing peak temperature for an effective time of 3 seconds. For samples passivated with AlO_x / SiN_x stack, firing is performed at a peak temperature of 880°C for an effective time of 3 seconds. Effective lifetime of the minority charge carriers (τ_{eff}) is measured in at least 10 positions of two

samples by quasi-steady-state photoconductance (QSSPC) method using Sinton WCT 120 lifetime tester. The effective surface recombination velocity (S_{eff}) for symmetrical test samples is then calculated using τ_{eff} as in [23].

$$S_{eff} = \frac{W}{2} \left[\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}} \right) - \left(\frac{W^2}{D_n \pi^2} \right) \right] \quad (3)$$

Where, bulk lifetime τ_{bulk} is obtained from a known value of τ_{SRH} and $\tau_{intrinsic}$ as per [24], W =thickness of the wafer, and D_n is diffusion constant of minority carriers calculated at 25°C.

Fig. 4 ii) plots the calculated S_{eff} for B-Si, mB-Si, and alkaline textured wafers. For the nanotextured wafers passivated with SiriON stack, we can see that the S_{eff} value is initially very high for B-Si wafers ($S_{eff} \approx 10^5$ cm/s). With an increasing surface modification time, a linear trend of decreasing S_{eff} can be seen. Since the S_{eff} is plotted in logarithmic scale, this suggests an exponential decrement of S_{eff} with an increasing surface modification time. Surface passivation improves slightly for mB-Si 1 ($S_{eff} \approx 10^4$ cm/s) and for mB-Si 2 ($S_{eff} \approx 10^3$ cm/s) whereas reduces to a low level for mB-Si 3 ($S_{eff} < 65$ cm/s, $S_{eff,min} \approx 14$ cm/s). For an equivalent surface passivation, S_{eff} for alkaline texture is slightly lower ($S_{eff} < 10$ cm/s) than mB-Si 3. Interestingly, nanotextured surfaces passivated with ALD AlO_x / PECVD SiN_x show much higher passivation level. An improvement in S_{eff} of about three orders of magnitude ($S_{eff} \leq 100$ cm/s) is observed for B-Si texture passivated with AlO_x / SiN_x stack in comparison to SiriON stack. Furthermore, again an exponential trend of decreasing S_{eff} is observed for an increasing surface modification time and both mB-Si 1 and mB-Si 2 reach good passivation level ($S_{eff} \leq 35$ cm/s). Especially, mB-Si 2 reaches an equivalent surface passivation to that of alkaline texture ($S_{eff,min} < 10$ cm/s). In summary, surface passivation of nanotextured surfaces with PECVD layer stacks reach an acceptable level only after a certain surface modification time whereas a large improvement in passivation can be achieved by the application of ALD AlO_x layer.

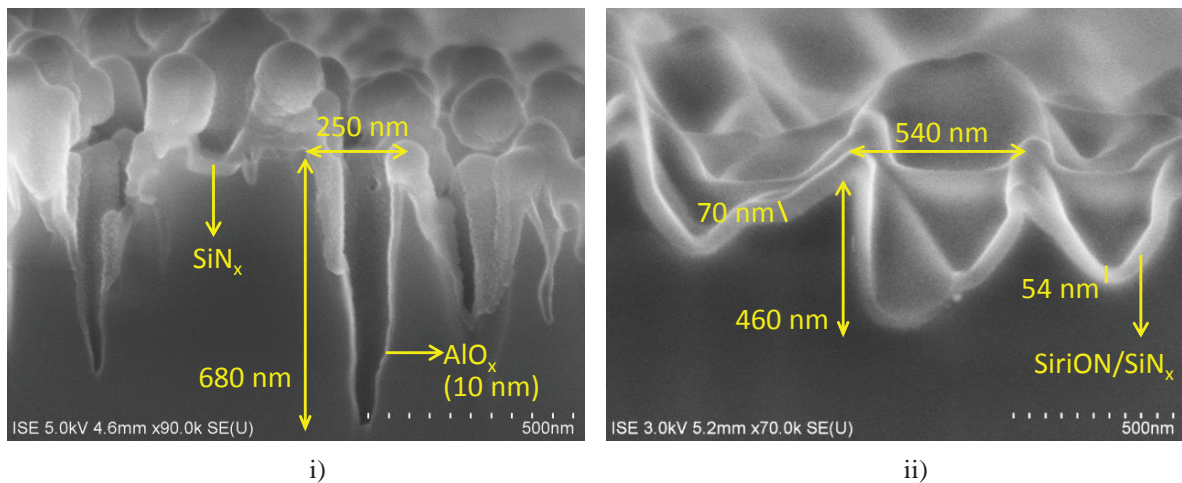


Fig. 5. SEM cross-sectional images of i) B-Si after passivation with ALD AlO_x / PECVD SiN_x stack, and ii) mB-Si 3 after passivation with PECVD SiriON / SiN_x stack.

In order to understand the problem, a close look to the passivation layer conformality is necessary. Fig. 5 i) shows a cross-sectional image of a B-Si wafer passivated with ALD AlO_x / PECVD SiN_x stack. The cross-sectional SEM image strongly suggests that the thin ALD AlO_x layer (≈ 10 nm) forms very conformal coating in the nanostructure geometry whereas PECVD SiN_x layer is deposited mostly on the top-section of the texture and the valleys remain un-passivated. Previous studies have also reported the non-conformal nature of PECVD deposited layers, especially on rough surfaces like that of B-Si [25,26]. The deposition of PECVD SiN_x occurs by the excitation of reactants (SiH_3 and NH_3) in the gas phase in order to deposit solid phase layers on the substrate. Therefore, a high aspect ratio

and narrow openings of a nanostructure can be expected to cause loss of conformability of PECVD deposited layers [25]. In contrast, ALD technique is known to deposit very conformal layers of well-defined thicknesses on rough surfaces [19,20,27] due to a separation of alternate cycles of precursor adsorption and oxidation steps that are both self-limiting in nature [27]. This leads to a very low passivation level of B-Si surfaces when only PECVD deposited layers are used for the surface passivation whereas the passivation dramatically improves by the deposition of a thin layer of ALD AlO_x . Surface modification process simultaneously changes the width and depth of nanostructures, which allows a more conformal deposition of passivation layers using standard deposition techniques like PECVD. Fig. 5 ii) shows a cross-sectional image of mB-Si 3 sample that is passivated by the PECVD deposited SiO_2 / SiN_x layer stack. In the course of surface modification process, B-Si texture changes into the nanotextured surface with structures of aspect ratios that are close to unity ($d \approx 500$ nm, $w \approx 500$ nm). This leads to the improvement in the conformal nature of the PECVD deposited layers and therefore allows a low S_{eff} value.

For the nanotextured samples passivated with AlO_x / SiN_x stack, an exponential decay trend of S_{eff} for an increasing surface modification time can therefore be attributed mostly to a reduction in overall surface area and possibly to the crystal-orientation dependent recombination property of the passivation layer. Although the samples passivated with SiO_2 / SiN_x also show an exponential decay trend, the decay constant is much larger than for the samples passivated with AlO_x / SiN_x and therefore cannot be explained only by a change in surface area ratio and crystal-orientation dependency of the passivation layer. In this case, formation of nanotexture not only increases the surface area by many folds, but also introduces a geometry-dependent recombination component that comes into play when the deposition method fails to form a conformal passivation layer.

3.2. Passivation of high-efficiency emitter for nanotextured surfaces

In this section, we perform a study of passivating n-type emitters on nanotextured and reference textured surfaces with PECVD and ALD based passivation techniques. Large area ($15.6 \times 15.6 \text{ cm}^2$) p-type CZ wafers ($4 \Omega \text{ cm}$, $200 \mu\text{m}$ thick) are used as test wafers. Modified nanostructures – mB-Si 1 ($R_w \approx 11 \%$) and mB-Si 3 ($R_w \approx 17 \%$) are formed after ADE nanotexturing and a subsequent post-etching process on both sides of the wafer. For reference, alkaline and acidic textured surfaces are also prepared.

We use POCl_3 -based tube diffusion process to form two different emitters – Emitter X and Emitter Y on the textured surfaces. In emitter X, it is intended to have a controlled reduction of inactive and active phosphorous concentration in the near-surface emitter region. Such an approach has previously led to the J_{sc} increment of 0.8 mA/cm^2 in mB-Si 3 based mc-Si solar cell in comparison to the acidic textured mc-Si solar cell whereas also allowing a high $FF > 80\%$ for a Al-BSF solar cell. We perform further optimization of the n-type emitter diffusion process by taking the following four factors into consideration: i) enough surface phosphorous concentration (N_{sh}) to allow low contact resistivity with screen-print; ii) low inactive N_{sh} to limit recombination in near-surface region; iii) reasonably low active doping concentration in emitter bulk to limit surface and Auger recombination; and iv) reasonably shallow emitter profile to increase the collection probability of the charge carriers that are generated in top-section of the nanotexture. Variation of the pre-deposition and drive-in parameters of the emitter diffusion process is performed in order to achieve a high-efficiency emitter – hereby called Emitter Y for the application in PERC-type mc-Si solar cells. A detailed description of the influence of diffusion parameters on the emitter characteristics is out of the scope of this paper and will be presented in future publications. Here, we mainly focus on the comparative study of the emitter passivation on newly developed mB-Si surfaces by PECVD and ALD based deposition methods.

After the PSG etching, both sides of wafers are either passivated by anti-reflective coating PECVD SiN_x or by a stack of ALD AlO_x and PECVD SiN_x to achieve reflection minimum near 600 nm . Fig. 6 i) shows the surface reflection for different textures in the spectral range of $250\text{-}1200 \text{ nm}$ after PECVD SiN_x deposition. Modified nanotexture samples show a much lower surface reflection value to the acidic texture in the wavelength spectrum of $250\text{-}1100 \text{ nm}$ suggesting that the reflection gain is not only in the UV region. mB-Si 1 show a much lower R_w in comparison to mB-Si 3 whereas very close to that of the reference alkaline texture.

After the surface passivation step, fast firing was performed at the peak wafer temperature of 840°C for 3 seconds and quasi steady state photo conductance (QSSPC) measurements were performed in generalized mode. Since we used low resistivity p-type wafers for the experiment, an accurate estimation of j_{oe} is difficult to achieve as described

in [28,29]. Therefore, we rather plot the implied V_{OC} ($V_{OC,impl}$) values extracted from the lifetime tester at 1 sun illumination as the measure of the emitter passivation level according to the following equation [30]:

$$V_{OC,impl} = \frac{k_B T}{q} \ln \left(\frac{(N_{dop} + \Delta n) \Delta n}{n_i^2} \right) \quad (4)$$

where, k_B is Boltzmann constant, T the temperature, N_{dop} the intrinsic doping level, q the elementary charge, Δn the injection density and n_i the intrinsic concentration.

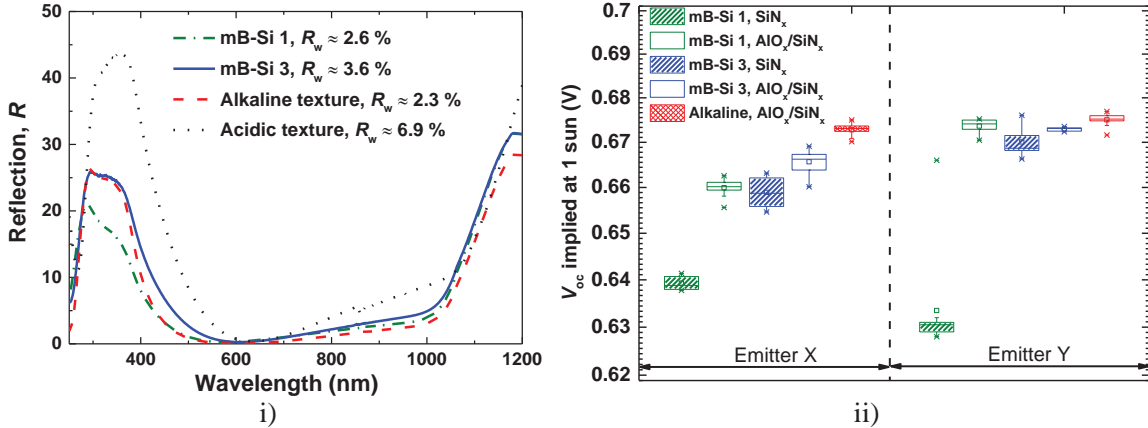


Fig. 6. i) Hemispherical surface reflection R and weighted surface reflection R_w for different surface textures on mono c-Si surfaces after deposition of PECVD SiN_x , ii) plot showing implied V_{OC} for nanotextured and reference textured surfaces after passivation of two different emitters – emitter X and emitter Y either by PECVD SiN_x or by ALD AlO_x / PECVD SiN_x layer stack and successive fast-firing step.

Fig. 6 ii) compares the $V_{OC,impl}$ for nanotextured surfaces and the reference alkaline textured surface for emitter X and emitter Y after passivation with PECVD SiN_x or with ALD AlO_x / PECVD SiN_x layer stack. We observe that regardless of the emitter diffusion process, mB-Si 1 deposited with PECVD SiN_x shows a poor passivation level. As soon as mB-Si 1 is passivated with AlO_x / SiN_x stack, the passivation level improves dramatically for both emitter diffusion processes. This suggests that surface passivation is the major limiting factor for the electrical performance of mB-Si 1 nanotexture. In contrast, regardless of the emitter diffusion process, only a slight difference in $V_{OC,impl}$ is observed for mB-Si 3 if AlO_x / SiN_x stack is used instead of SiN_x layer. As discussed in section 3-3.1, a longer post-etching time not only decreases the S_f of the nanotexture (see Fig. 2 ii), but also allows a conformal deposition of the PECVD-based passivation layer (see Fig. 5). This leads to overall higher $V_{OC,impl}$ values for mB-Si 3 samples in comparison to that of mB-Si 1 samples if PECVD SiN_x is used as surface passivation layer.

The $V_{OC,impl}$ of nanotextured surfaces is, however, still lower in comparison to the reference alkaline textured surface for emitter X. This suggests a higher recombination in emitter region of nanotextured surfaces in comparison to the reference textured surface. For emitter X, a lower $V_{OC,impl}$ of mB-Si 1 in comparison to mB-Si 3 after passivation with AlO_x / SiN_x suggests an overall higher emitter recombination in mB-Si 1. Nevertheless, after the application of our newly developed emitter diffusion process (emitter Y), the $V_{OC,impl}$ values for mB-Si 1 with AlO_x / SiN_x stack reaches the same level to that of mB-Si 3 passivated with either of SiN_x or AlO_x / SiN_x layer stack and alkaline texture passivated with AlO_x / SiN_x layer stack. This suggests that diffusion of emitter Y significantly decreases the recombination in the emitter region of nanotexture in comparison to emitter X. Eventually, we have managed to reach low contact resistivity ($\rho_c < 5 \text{ m } \Omega \text{ cm}^2$) on nanotextured surfaces for both emitter X and emitter Y after screen-print metallization and fast firing processes. This opens the possibility of fabricating high-efficiency nanotextured mc-PERC type Si solar cells.

4. Summary

F₂-based nanotexturing approach can form B-Si texture with very low surface reflection properties, which however also leads to high surface recombination related losses. A simple post-etching step can be used to change the geometry of the B-Si to form mB-Si texture. A gradual decrease in S_{eff} and an increase in surface reflection of mB-Si texture are observed with an increasing duration of the surface modification process. mB-Si samples formed after varying surface modification times are used to study the influence of the post-etching process on the electrical properties of the respective samples. For the deeper nanotexture (mB-Si 1), a failure of forming a conformal passivation layer by PECVD process introduces a geometry dependent recombination factor and surface recombination is the dominant recombination mechanism. Excellent surface passivation of mB-Si with PECVD layers can be achieved by prolonging the post-etching process duration to form shallower texture -mB-Si 3 ($S_{\text{eff,min}} \approx 14 \text{ cm/s}$), whereas still allowing a reasonably low surface reflection after anti-reflection coating ($R_w < 4 \%$). If an ALD based passivation method is applied, even the deeper nanotextures can be passivated to reach high passivation levels ($S_{\text{eff}} \leq 35 \text{ cm/s}$ for mB-Si 1 and $S_{\text{eff}} \leq 10 \text{ cm/s}$ for mB-Si 2 and mB-Si 3). An effective suppression of recombination in both surface and the emitter region is required in order to reach a high passivation level in the nanotextured surfaces diffused with n-type emitter. We show that a further reduction in emitter related recombination loss leads to mB-Si surfaces reaching an equivalently high passivation level ($V_{\text{OC,impl}} \geq 670 \text{ mV}$) and low contact resistivity ($\rho_c < 5 \text{ m}\Omega \text{ cm}^2$) to that of reference textured surfaces. These results have paved the way towards high efficiency nanotextured PERC-type solar cells on mc-Si substrates.

Acknowledgements

The authors would like to thank Jutta Zielonka for SEM measurements and to all colleagues in PVTEC lab in Fraunhofer ISE for processing of the samples. B. Kafle gratefully acknowledges Rosa Luxemburg Foundation for the financial support provided during his PhD studies.

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